

**Programmable Voltage Controlled Oscillator (VCXO)**
**OUTPUT: LV-PECL**
**VG7050ECN**

- Frequency range : 50 MHz to 800 MHz  
(Tuning resolution:  $2.2 \sim 2.8 \times 10^{-9}$ )
- Supply voltage : 2.5 V / 3.3 V
- External dimensions :  $7.0 \times 5.0 \times 1.5$  mm (10 pins)
- Absolute Pull Range :  $\pm 0$  to  $\pm 180 \times 10^{-6}$  (12 steps selectable)

**Features**

- User-specified four startup frequency, APR and 7-bit I<sup>2</sup>C address
- User Programming : I<sup>2</sup>C Interface
- Low jitter PLL technology

**Applications**

SONET/SDH, OTN, GbE, Fibre Channel

\*The I2C-Bus is a trademark of NXP Semiconductors


**Product Number (please contact us)**  
**X1G004561xxxx00**


Actual size


**Specifications (characteristics)**

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	f <sub>o</sub>	50 MHz to 800 MHz	It can be changed by I <sup>2</sup> C
Supply voltage	V <sub>CC</sub>	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.33 V	
Storage temperature	T <sub>stg</sub>	-55 °C to +125 °C	Storage as single product
Operating temperature	T <sub>use</sub>	-40 °C to +85 °C	
Frequency tolerance *1	f <sub>tol</sub>	±50 × 10 <sup>-6</sup> Max.	Includes frequency aging (10 years)
Current consumption	I <sub>CC</sub>	90 mA Max.	OE Active, L_ECL=50 Ω
Disable current	I <sub>dis</sub>	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Absolute pull range	APR	±0 to ±180 × 10 <sup>-6</sup>	V <sub>c</sub> = 1.65 V ± 1.35 V (V <sub>CC</sub> = 3.3 V)
		±0 to ±180 × 10 <sup>-6</sup>	V <sub>c</sub> = 1.25 V ± 1.00 V (V <sub>CC</sub> = 2.5 V)
Control voltage tuning range	V <sub>c</sub>	0 to V <sub>CC</sub>	
Frequency change polarity	-	Positive slope	0 to V <sub>CC</sub>
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V <sub>OH</sub>	V <sub>CC</sub> -1.025 V Min.	DC characteristics
	V <sub>OL</sub>	V <sub>CC</sub> -1.62 V Max.	
Output load condition	L_ECL	50 Ω	Termination to V <sub>CC</sub> - 2.0 V
Input voltage	V <sub>IH</sub>	70% V <sub>CC</sub> Min.	OE, FSEL0, FSEL1, SDA and SCL
	V <sub>IL</sub>	30% V <sub>CC</sub> Max.	
Rise time / Fall time	t <sub>r</sub> /t <sub>f</sub>	400 ps Max.	Between 20% and 80% of (V <sub>OH</sub> -V <sub>OL</sub> )
Start-up time	t <sub>str</sub>	10 ms Max.	Time at minimum supply voltage to be 0 s

\*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

 Product name **VG7050 ECN SM20xxxx** C J G H P Z  
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

- ① Model
- ② Output (E: LV-PECL)
- ③ Parameter Designator (VG7050ECN: SM20xxxx)
- ④ Supply voltage (C: 3.3 V Typ., D: 2.5 V Typ.)
- ⑤ Frequency tolerance (J:  $\pm 50 \times 10^{-6}$ )
- ⑥ Operating temperature (G: -40 ~ +85°C)
- ⑦ OE Function (H: Active High, L: Active Low)
- ⑧ Absolute Pull Range (P: Programmable)
- ⑨ Output Standby Type (F: Fix (OUT="L", OUTN="H"), Z: High-Z)

**Phase Jitter**

	Offset Frequency	125.00 MHz	156.25 MHz	250.00 MHz	425.00 MHz	622.08 MHz	669.33 MHz	794.73 MHz
Phase jitter*2 Typ.	12 kHz to 20 MHz	0.30 ps	0.26 ps	0.26 ps	0.25 ps	0.26 ps	0.26 ps	0.26 ps
	20 kHz to 50 MHz	0.30 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps
	50 kHz to 80 MHz	0.29 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps

 \*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μF + 10 μF) between V<sub>CC</sub> and GND pin should be placed as close to the V<sub>CC</sub> pin as possible.

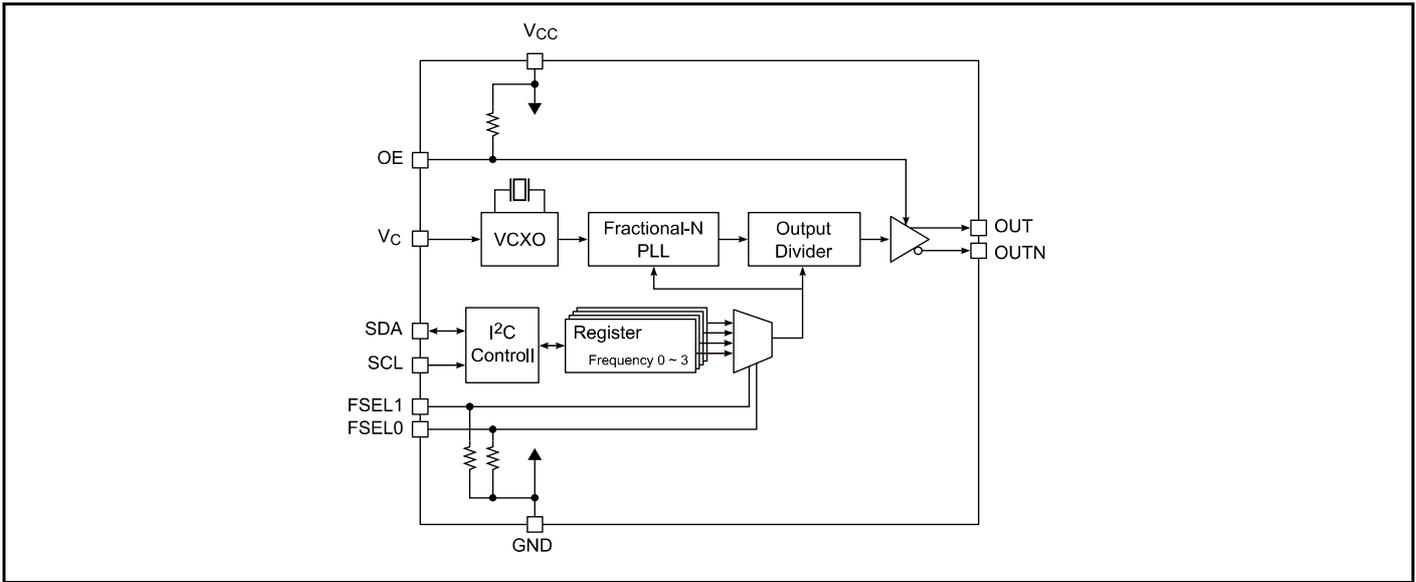
SHENZHEN YIJIN ELECTRONICS CO: LTD TEL: 0755-27876565

18924600166

QQ: 857950243

<http://www.vc-tcxo.com>

Block diagram

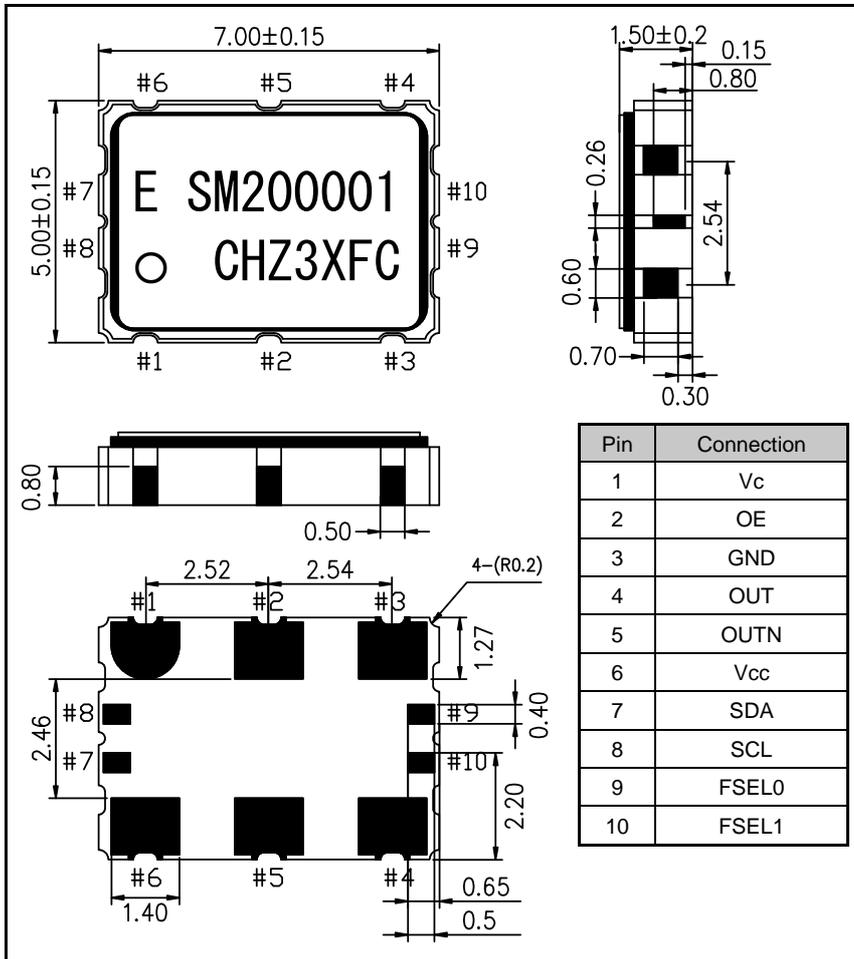


OE Function / OE Standby Type

OE Function	OE Standby Type	Frequency output OE pin	Oscillator Stop	
			OE pin	OUT,OUTN state
H: Active High	Z: High-Z	"H" or "OPEN"	"L"	High Impedance
L: Active Low		"L" or "OPEN"	"H"	
H: Active High	F: Fix	"H" or "OPEN"	"L"	OUT="L", OUTN="H"
L: Active Low		"L" or "OPEN"	"H"	

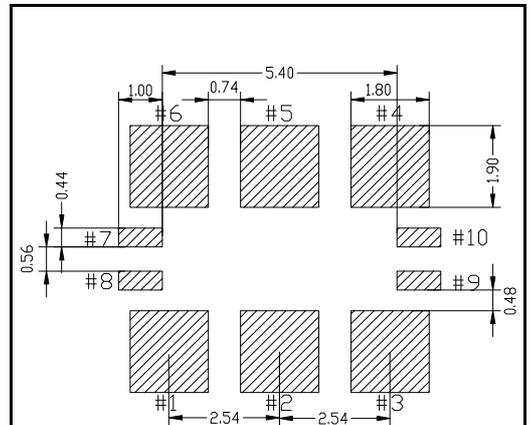
External dimensions

(Unit: mm)



Footprint (Recommended)

(Unit: mm)



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1  $\mu$ F + 10  $\mu$ F) between VCC and GND pin should be placed as close to the VCC pin as possible.

## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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	► Pb free.
	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
	► Designed for automotive applications related to driving safety (Engine Control Unit, Air Bag, ESC etc.)

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